PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13
Req for Recon.
J. McMillan
4/1/03

In re the Application of:

HIRANO et al.

Art Unit: 2811

Application No.: 09/813,866

Examiner: S. Gebremariam

Filed: March 22, 2001

Attorney Dkt. No.: 107318-00000

For: SEMICONDUCTOR DEVICE DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

REQUEST FOR RECONSIDERATION UNDER 37 CFR § 1.121

Commissioner for Patents
Washington, D.C. 20231

March 24, 2003

Sir:

The Office Action dated October 23, 2002, has been received and carefully noted. The period for response having been extended from January 23, 2003 to March 24, 2003 (March 23, 2003 being a Sunday), by the attached Petition for Extension of Time, the following remarks are submitted as a full and complete response thereto.

Claims 60-69 are pending in the present application, and therefore, are respectfully submitted for reconsideration.

Claims 60, 61 and 63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 5,854,096, hereinafter "Ohtani") in view of Hashizume (JP 40328651A). In making this rejection, the Office Action took the position that Ohtani discloses all of the elements of the claimed invention with the exception of showing the method of using a light source emitting sheet-type annealing

light in order to activate the impurity region and crystallizing the amorphous silicon. The Office Action cites Hashizume for curing the deficiencies that exist in Ohtani. Applicants respectfully traverse this rejection, and submit that each of claims 60, 61 and 63 recite subject matter that is neither disclosed nor suggested in the cited prior art.

It is noted that claims 66-69 were not specifically rejected in the Office Action. However, Applicants shall address and respond to the comments made with respect to claims 66-69 within the Office Action.

Claim 60 recites a method of fabricating a semiconductor device. The method includes the steps of forming an amorphous silicon film on a substrate, heat treating the amorphous silicon film by laser annealing, therein forming a polycrystalline silicon film, and forming an impurity region in the polycrystalline silicon film. In addition, the steps include rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region.

Claim 66 recites a method of fabricating a semiconductor device. The method includes the steps of forming an amorphous silicon film on a substrate, heat treating the amorphous silicon film by laser annealing performed by applying a laser beam in the form of a sheet, therein forming a polycrystalline silicon film, and forming an impurity region in the polycrystalline silicon film. Furthermore, the steps include rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region.

Accordingly, the essence of the present invention is a method of fabricating a semiconductor device having at least the step of rapidly heat treating the impurity region

by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region. As such, the present invention results in the advantage of improving the throughput in fabricating a thin film transistor or a liquid crystal display by fabricating a high-quality polycrystalline silicon film in a reduced time.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 60 and 66, and therefore, fails to provide the advantages which are provided by the present invention.

Ohtani discloses a process for fabricating a semiconductor device having the steps of introducing into an amorphous silicon film, a metallic element which accelerates the crystallization of the amorphous silicon film, and applying heat treatment to the amorphous silicon film to obtain a crystalline silicon film. In addition, Ohtani discloses the steps of irradiating a laser beam or an intense light to the crystalline silicon film, and heat treating the crystalline silicon film irradiated with a laser beam or an intense light.

Hashizume discloses irradiating a thin semiconductor film with a sheet-type annealing light to anneal a silicon layer in order to obtain a silicon layer whose physical properties and qualities are good. The light source disclosed in Hashizume is a laser beam. In order to anneal the whole surface of a glass substrate 31, the laser beam is scanned at the rate of 1 mm/s in the Y-direction. The width of the laser beam in the X-direction may be adjusted by changing the relative positions of the lenses. The energy density of the laser beam is adjusted by adjusting the distance between the specimen and the convex lens closest to the specimen.

Applicants respectfully submit that each and every element recited within claims 60 and 66 is neither disclosed nor suggested by Ohtani and/or Hashizume, taken alone or in combination. In particular, Applicants respectfully submit that the method of fabricating a semiconductor device as recited in the present application is clearly distinct from that which is illustrated by the combination of Ohtani and/or Hashizume. Specifically, it is respectfully submitted that the cited prior art fails to disclose or suggest the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region.

Although Ohtani discloses a process for fabricating a semiconductor device having the two-step crystallization process of heat treatment followed by major annealing, Applicants nevertheless submit that Ohtani fails to disclose or suggest the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region. Furthermore, Hashizume merely discloses a method of irradiating a semiconductor film with a sheet-type annealing light to anneal a silicon layer in order to obtain a silicon layer whose physical properties and qualities are good. It is submitted that nowhere in Hashizume discloses or suggests the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region. Accordingly, Applicants respectfully submit that neither Ohtani and/or Hashizume, taken alone or in combination, disclose or suggest each and every element recited within claims 60 and 66 of the present application.

As for claims 61, 63, 67, and 69, Applicants submit that each of these claims recites subject matter which is neither disclosed nor suggested by the cited prior art. In particular, each of these claims depends on claims 60 and 66, respectively. Therefore, each of claims 61, 63, 67 and 69 incorporates each and every limitation recited within claims 60 and 66, respectively therein. Therefore, Applicants submit that each of these claims also recite subject matter that is neither disclosed nor suggested by Ohtani and/or Hashizume, taken alone or in combination, for at least the reasons set forth above with respect to claims 60 and 66.

Claims 62 and 68 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohtani in view of Hashizume and further in view of Tajima (JP 02194626). In making this rejection, the Office Action took the position that the combination of Ohtani and Hashizume discloses all of the elements of the claimed invention with the exception of showing a xenon arc lamp that is employed in the light source. The Office Action cites Tajima for curing the deficiencies that exist in the combination of Ohtani and Hashizume. Applicants respectfully traverse this rejection, and submit that each of claims 62 and 68 recite subject matter that is neither disclosed nor suggested in the cited prior art.

Tajima discloses the process of heat treating a semiconductor device after ion implantation for forming source-drain regions by irradiating the semiconductor with light rays from a xenon arc lamp. The majority of the light from the xenon arc lamp contains wavelengths shorter than 1 μm. Thus, the absorption efficiency of these wavelengths by Si is high. This high absorption efficiency reduces the heat treatment time.

Applicants respectfully submit that each and every element recited within claims 62 and 68 is neither disclosed nor suggested by the combination of prior art references. In particular, each of claims 62 and 68 depends from independent claims 60 and 66, respectively. Therefore, each and every limitation recited within claims 60 and 66 is also recited within claims 62 and 68, respectively. Accordingly, each of claims 62 and 68 includes at least the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region. As mentioned above, Tajima merely discloses the process of heating a thin-film conductor film to enable heat treatment at high temperature and to improve the crystal properties by carrying out this heat treatment through irradiation of light rays from a short wave length arc lamp. It is submitted that Tajima fails to disclose or suggest the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region. Accordingly, it is respectfully submitted that Tajima fails to cure the deficiencies which exist in the combination of Ohtani and Hashizume. As such, Applicants respectfully submit that Ohtani, Hashizume, and/or Tajima, taken alone or in combination, fail to disclose or suggest each and every element recited within claims 62 and 68 of the present application.

Claims 64 and 65 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohtani in view of Hashizume and further in view of Rohatgi et al. (U.S. Patent No. 5,766,9644, hereinafter "Rohatgi"). In making this rejection, the Office Action took the position that the combination of Ohtani and Hashizume discloses all of the elements of

the claimed invention with the exception of showing rapid thermal annealing that is performed a plurality of times, and showing the heating temperature being increased stepwise from an initial time to a final time. The Office Action cites Rohatgi for curing the deficiencies which exist in the combination of Ohtani and Hashizume. Applicants respectfully traverse this rejection, and submit that each of claims 64 and 65 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Rohatgi discloses processes which utilize rapid thermal processing (RTP) for inexpensively producing high efficiency silicon solar cells. The RTP processes preserve minority carrier bulk light time τ and permits selected adjustment of the depth of the diffused regions, including emitter and back surface field, within the silicon substrate.

Applicants respectfully submit that each and every element recited within claims 64 and 65 is neither disclosed nor suggested by Ohtani, Hashizume, and/or Rohatgi, taken alone or in combination. In particular, each of claims 64 and 65 depends from independent claim 60. Therefore, each and every limitation recited within claim 60 is also recited within claims 64 and 65. Accordingly, each of claims 64 and 65 also include at least the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region. As mentioned above, Rohatgi merely discloses processes for producing low cost, high efficient solar cells using the rapid thermal processing. It is submitted that Rohatgi fails to disclose or suggest the step of rapidly heat treating the impurity region by rapid thermal annealing using a light source emitting sheet-type annealing light, therein activating the impurity region, and therefore Rohatgi fails to cure

the deficiencies which exist in the combination of Ohtani and Hashizume. As such, Applicants respectfully submit that Ohtani, Hashizume, and/or Rohatgi, taken alone or in combination, fails to disclose or suggest each and every element recited within claims 64 and 65 of the present application.

In view of the above, Applicants respectfully submit that claims 60-69 each recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art and, therefore, respectfully request that claims 60-69 be found allowable and that this application be passed to issue.

If for any reasons, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to

Counsel's Deposit Account 01-2300, referring to Attorney Docket number 107318-00000.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (two months)
Associate Power of Attorney